WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor element, the semiconductor element having at least a substrate, a lower wiring, an upper wiring layer, a via-hole connecting the lower wiring layer to the upper wiring layer, and a W material filled in the via-hole, the method comprising:

forming the lower wiring layer on top of the substrate;

forming the via-hole to extend upwardly from the lower wiring layer;

feeding a fluorine compound gas having a reducing function into the via-hole;

forming a W nucleus in the via-hole;

filling the via-hole with W; and

forming the upper wiring layer.

2. The method of manufacturing a semiconductor element according to Claim 1, wherein the fluorine compound gas has a cleaning function.

3. The method of manufacturing a semiconductor element according to Claim 1, wherein the fluorine compound gas includes a WF_6 gas.

4. The method of manufacturing a semiconductor element according to Claim 1, wherein the fluorine compound gas includes a NF_3 gas.

5. The method of manufacturing a semiconductor element according to Claim 1, wherein the fluorine compound gas includes a SiF_4 gas.

6. A method of manufacturing a semiconductor element,

the semiconductor element having at least a substrate, a lower wiring, an upper wiring layer, a via-hole connecting the lower wiring layer to the upper wiring layer, and a W material filled in the via-hole, the method comprising:

forming the lower wiring layer on top of the substrate;

forming the via-hole to extend upwardly from the lower wiring layer;

feeding a fluorine compound gas into the via-hole to clean the via-hole and form a part of a W nucleus in the via-hole, the fluorine compound gas having a reducing function and a cleaning function;

forming the remainder of the W nucleus;

filling the via-hole with W; and

forming the upper wiring layer.

7. The method of manufacturing a semiconductor element according to Claim 6, wherein the fluorine compound gas includes a SiF_4 gas.

8. A method of manufacturing a semiconductor element, the semiconductor element having at least a substrate, a lower wiring, an upper wiring layer, a via-hole connecting the lower wiring layer to the upper wiring layer, and a W material filled in the via-hole, the method comprising:

forming the lower wiring layer on top of the substrate;

forming the via-hole to extend upwardly from the lower wiring layer;

feeding a fluorine compound gas into the via-hole to clean the via-hole and form a part of a W nucleus in the

via-hole, the fluorine compound gas having a reducing function and a cleaning function;

feeding a SiH_4 gas and a WF_6 gas into the via-hole to form the remainder of the W nucleus;

filling the via-hole with W by a CVD process; and

forming the upper wiring layer.

9. The method of manufacturing a semiconductor element according to Claim 1, wherein the filling of the via-hole with W is performed by a CVD process.

10. The method of manufacturing a semiconductor element according to Claim 1, wherein the forming of a W nucleus includes feeding a SiH4 gas and a WF6 gas into the via-hole.

11. The method of manufacturing a semiconductor element according to Claim 1 further comprising forming a first insulation layer between the substrate and the lower wiring layer.

12. The method of manufacturing a semiconductor element according to Claim 11 further comprising forming a second insulation layer between the lower wiring layer and the upper wiring layer, wherein the via-hole extends into the second insulation layer.

13. The method of manufacturing a semiconductor element according to Claim 1 further comprising performing a sputtering process and forming an adhesive layer on the via-hole, between the forming of the via-hole and the feeding of the fluorine compound.

14. The method of manufacturing a semiconductor element according to Claim 6, wherein the filling of the via-hole with W is performed by a CVD process.

15. The method of manufacturing a semiconductor element according to Claim 6, wherein the forming the remainder of the W nucleus includes feeding a SiH4 gas and a WF6 gas into the via-hole.

16. The method of manufacturing a semiconductor element according to Claim 6 further comprising forming a first insulation layer between the substrate and the lower wiring layer.

17. The method of manufacturing a semiconductor element according to Claim 16 further comprising forming a second insulation layer between the lower wiring layer and the upper wiring layer, wherein the via-hole extends into the second insulation layer.

18. The method of manufacturing a semiconductor element according to Claim 6 further comprising performing a sputtering process to clean the via-hole and forming an adhesive layer on the via-hole, between the forming of the via-hole and the feeding of the fluorine compound.

19. The method of manufacturing a semiconductor element according to Claim 6, wherein the part of the W nucleus formed by the fluorine compound gas is a Si layer.

20. The method of manufacturing a semiconductor element according to Claim 8 further comprising performing a sputtering process to clean the via-hole and forming an

adhesive layer on the via-hole, between the forming of the via-hole and the feeding of the fluorine compound.